have a height from about 10 nm to about 500 nm. The semiconductor strips **24** may have a width from about 5 nm to 50 nm. The semiconductor strips **24** may have a length from about 0.01 um to 10 um. In an alternative embodiment, the semiconductor strips **24** may be epitaxially grown from a top surface of the semiconductor substrate **20** within trenches or openings formed in a patterned layer (e.g. the dielectric layer **22**) atop the semiconductor substrate **20**. Because the process is known in the art, the details are not repeated herein.

The semiconductor strips **24** may be formed of semiconductor material such as silicon, germanium, silicon germanium, or the like. In an embodiment, the semiconductor strips **24** are silicon. The semiconductor strips **24** may then doped through an implantation process to introduce p-type or n-type impurities into the semiconductor strips **24**.

The dielectric layer **22** may blanket deposited on the FinFET device **100**. The dielectric layer **22** may be made of one or more suitable dielectric materials such as silicon oxide, silicon nitride, low-k dielectrics such as carbon doped oxides, extremely low-k dielectrics such as porous carbon doped silicon dioxide, a polymer such as polyimide, combinations of these, or the like. The dielectric layer **22** may be deposited through a process such as chemical vapor deposition (CVD), or a spin-on-glass process, although any acceptable process may be utilized.

After the dielectric layer **22** is deposited, the dielectric layer **22** may be planarized to level a top surface of dielectric layer **22** and top surfaces of a hard mask layer (not shown in FIGS. **2**A and **2**B) on the tops of the semiconductor strips **24**. The hard mask layer may be removed by an etch process comprising H_3PO_4 or the like. The dielectric layer **22** may be planarized in a variety of ways. In an embodiment, the planarization process involves a chemical mechanical polishing (CMP), in which the dielectric layer **22** is reacted and then ground away using an abrasive. This process may continue until the tops of the semiconductor strips **24** are exposed. In another embodiment, the dielectric layer **22** may be thinned by a diluted hydrofluoric acid (DHF) treatment or a vapor hydrofluoric acid (VHF) treatment for a suitable time.

After the dielectric layer **22** is planarized, a gate **32** may be formed over the semiconductor strips **24** and the dielectric layer **22**. The gate **32** may include a gate dielectric layer **26** and gate spacers **34**. The gate dielectric layer **26** may be formed by thermal oxidation, CVD, sputtering, or any other methods known and used in the art for forming a gate dielectric. In other embodiments, the gate dielectric layer **26** includes dielectric materials having a high dielectric constant (k value), for example, greater than 3.9. The materials may include silicon nitrides, oxynitrides, metal oxides such as HfO_2, $HfZrO_x$, $HfSiO_x$, $HfTiO_x$, $HfAlO_x$, the like, or combinations and multi-layers thereof.

The gate electrode layer (not shown) may be formed over the gate dielectric layer **26**. The gate electrode layer may comprise a conductive material and may be selected from a group comprising polycrystalline-silicon (poly-Si), polycrystalline silicon-germanium (poly-SiGe), metallic nitrides, metallic silicides, metallic oxides, and metals. The gate electrode layer may be deposited by CVD, sputter deposition, or other techniques known and used in the art for depositing conductive materials. The top surface of the gate electrode layer usually has a non-planar top surface, and may be planarized prior to patterning of the gate electrode layer or gate etch. Ions may or may not be introduced into the gate electrode layer at this point. Ions may be introduced, for example, by ion implantation techniques. The gate electrode layer and the gate dielectric layer may be patterned to form the gate **32**. The gate patterning process may be accomplished by depositing mask material (not shown) such as photoresist or silicon oxide over the gate electrode layer. The mask material is then patterned and the gate electrode layer is etched in accordance with the pattern.

Gate spacers **34** may be formed on opposite sides of the gate **32**. The gate spacers **34** are typically formed by blanket depositing a spacer layer (not shown) on the previously formed structure. In an embodiment, the gate spacers **34** may include a spacer liner **31**. The spacer liner **31** may comprise SiN, SiC, SiGe, oxynitride, oxide, combinations thereof, or the like. The spacer layer may comprise SiN, oxynitride, SiC, SiON, oxide, combinations thereof, or the like and may be formed by methods utilized to form such a layer, such as CVD, plasma enhanced CVD (PECVD), low pressure CVD (LPCVD), atomic layer deposition (ALD), sputter, and other methods known in the art. The gate spacers **34** are then patterned, preferably by anisotropically etching to remove the spacer layer from the horizontal surfaces of the structure.

FIGS. **3**A and **3**B illustrate the etching of portions of the semiconductor strips **24** in a strained source drain (SSD) etch step to form recesses **36** in the semiconductor strips **24**. The SSD etch may selectively etch the semiconductor strips **24** without etching the dielectric layer **22** or the gate **32** and gate spacers **34**. In an embodiment, the recesses **36** may be etched to have a depth from about 5 nm to about 25 nm. The SSD etch step may performed in a variety of ways. In an embodiment, the SSD etch step may be performed by a dry chemical etch with a plasma source and an etchant gas. The plasma source may be an inductively coupled plasma (ICR) etch, a transformer coupled plasma (TCP) etch, an electron cyclotron resonance (ECR) etch, a reactive ion etch (RIE), or the like and the etchant gas may be fluorine, chlorine, bromine, combinations thereof, or the like. In another embodiment, the SSD etch step may be performed by a wet chemical etch, such as ammonium peroxide mixture (APM), NH_4OH, TMAH, combinations thereof, or the like. In yet another embodiment, the SSD etch step may be performed by a combination of a dry chemical etch and a wet chemical etch.

After the recesses **36** are formed, the source regions **30** and drain regions **28** may be formed in the recesses **36** as illustrated in FIGS. **4**A and **4**B. The source regions **30** and the drain regions **28** may be formed by epitaxially growing SiGe, Si, SiP, combinations thereof, or the like in the recesses **36** with an optional cap layer of Si over the source regions **30** and the drain regions **28**. The epitaxial growth of the source regions **30** and the drain regions **28** forms a same crystalline orientation in the semiconductor strip **24**, the source regions **30**, and the drain regions **28**. The growth of the source regions **30** and the drain regions **28** may be substantially confined by the dielectric layer **22**. As illustrated in FIG. **4**B, sidewalls of the drain regions **28** may be substantially orthogonal to the top surface of the semiconductor substrate **20** and a top surface of the drain regions **28** may substantially parallel with the top surface of the semiconductor substrate **20**. In an embodiment, the top surface of the drain regions **28** may be substantially coplanar with a top surface of the dielectric layer **22**. In another embodiment, the top surface of the drain regions **28** may be below or above the top surface of the dielectric layer **22**. Although FIG. **4**B only illustrates the drain regions **28**, the source regions **30** have a similar structural configuration on an opposite side of gate **32** such that the description of the drain regions **28** is applicable to the source regions **30** as well.